VITA of Dr . ATHANASIOS (THANOS) STOURAITIS

CONTACT DETAILS

ECE Department
Khalifa University
PO Box 127788
Abu Dhabi, UAE
Email: thanos.stouraitis@kustar.ac.ae

ACADEMIC BACKGROUND

- PhD, Electrical Engineering, University of Florida, 1986.
- MS, Electrical & Computer Engineering, University of Cincinnati, 1983.
- MS, Electronic Automation, University of Athens, Greece, 1981.
- BS, Physics, University of Athens, Greece, 1979.

CURRENT RESEARCH INTERESTS

- Signal and image processing systems
- Cryptographic systems
- Computer arithmetic systems (LNS, RNS, etc.)
- Design and architecture of optimal digital systems

PROFESSIONAL EXPERIENCE

- President, IEEE Circuits and Systems Society, 2012-2013.
- Board of Governors, University of Sterea Hellas, 2003-6.
- Member, Univ. of Patras IT Scientific Board.
- Visiting Professor of Electrical Engineering and ICICS, University of British Columbia, Vancouver, BC, Canada, 2012.
- Founding Director, "Graduate Program on Signal Processing and Communications: Theory, Implementations, and Applications." (With the participation of European and American Universities), 1998-2015.
- Director, Digital Signal and Image Processing Lab, ECE Dept. Univ. of Patras, 1990-2015.
- Visiting Professor of Electrical Engineering, Polytechnic University, Brooklyn, NY, 2001-2.
- Director, Electronics and Computers Division, Electrical and Computer Engineering Department, University of Patras, 2000-2001.
- Professor of Electrical and Computer Engineering, University of Patras, April 1998-2015.
- Associate Professor of Electrical and Computer Engineering, University of Patras, 1993-1998.
- Assistant Professor of Electrical and Computer Engineering, University of Patras, 1990-1993
- Assistant *Professor* of Elecrical Engineering, The Ohio State University, 1987-1990.
- Visiting Assistant Professor of Electrical Engineering, University of Florida, 1986-1987.
- Teaching and *Research Assistant* of Electr. Engineering, Univ. of Florida, 1983-1986.
- Teaching and Research Assistant of Electr. Engineering, Univ. of Cincinnati, 1981-1983.
- Technical Manager, The Athena Group Inc., 1986-1987.
- Researcher of High Speed Digital Architecture Lab, HSDAL, University of Florida, 1983-7.
- Researcher of the National Electrical Manufacturers Association (NEMA) Laboratories, Cincinnati, Ohio, 1982-1983.

PROFESSIONAL ACTIVITIES AND AWARDS

1. *Fellow* of IEEE for contributions in "high-performance digital signal processing architectures and computer arithmetic."
2. *President, IEEE Circuits and Systems Society, 2012-2013.*
3. *Founding Director*, "*Graduate Program on Signal Processing and Communications: Theory, Implementations, Applications.*" (With the participation of European and American Universities), 1998-2015.
4. *Board of Governors of the University of Sterea Hellas*, member, 2003-4.
5. *President-Elect, IEEE Circuits and Systems Society, 2011*.
6. *Vice President, Conferences, IEEE Circuits and Systems Society, 2008-2010.*
7. *Member of the Board of Governors of IEEE Circuits and Systems Society, 2006-2009.*
8. *Director,* Electronics and Computers Division, Electrical and Computer Engineering Department, University of Patras, 2000-2001.
9. *Chair, Univ. of Patras/Chinese University of Defense Technology Collaboration Committee*, 2014
10. *Member of the Univ. of Patras Networks Board.*
11. *Chair of the Long-Term Strategy Committee of the IEEE Circuits and Systems Society, 2007.*
12. *2000 IEEE Circuits and Systems Society Guillemin-Cauer (best paper in all the Society's Transactions for 2 years) Award* for "Multifunction Architectures for RNS Processors," IEEE Transactions on Circuits and Systems, Part II: Analog and Digital Signal Processing, vol. 46, no. 8, pp. 1041-1054, August 1999.
13. MEDCHIP Project-VLSI Design Contest 1997 Award. *Faculty Supervisor*, Won for "A New Architecture for High-Precision Subtraction in LNS"
14. *Best Paper Award* "A new approach to elliptic curve cryptography: an RNS architecture," *IEEE Mediterranean Electrotechnical Conference (MELECON) 2006,* 16-19 May 2006. (Schinianakis, D., Kakarountas, A.P., Stouraitis, T.).
15. *General Chair of Conferences*
    - IEEE International Symposium on Communications, Control, and Signal Processing (ISCCSP) 2014, Athens, Greece
    - 17th IEEE Int. Conference on Electronics Circuits and Systems (ICECS 2010), Athens, Greece, Dec. 12-15, 2010.
    - IEEE CASS International Forum on Emerging and Selected Areas (CAS-FEST 2010) 2010, Athens, Greece, Dec. 12, 2010.
    - IEEE International Symposium on Wireless Pervasive Computing (ISWPC) 2008, Santorini, Greece.
    - IEEE International Symposium on Circuits and Systems (ISCAS) 2006, Kos, Greece
    - IEEE International Workshop on Signal Processing Systems (SiPS) 2005, Athens, Greece
    - 3rd IEEE Int. Conference on Electronics, Circuits, and Systems (ICECS '96), Rodos, Greece, October 13-16 1996
    - Technopolis '95, Univ. of Patras, December 1995.
16. *Chair, Technical Program Committee*
    - 6th IEEE Int. Conference on Electronics Circuits and Systems (ICECS'99), Pafos, Cyprus, September 1999.
    - VLSI Track, IEEE Int. Symp. On Circuits and Systems (ISCAS'00), Geneva, Switzerland, May 00.
    - 1998 European Signal Processing Conference, (Eusipco '98), Rodos, Greece, September 1998.
17. *Member of Technical Committees* of the IEEE Society of Circuits and Systems:
    - VLSI Systems and Applications (VSA), *Secretary, 1996-1998, Chair, 1998-2000*
    - Digital Signal Processing
    - Multimedia
18. *Editor*, Journal of Circuits, Systems, and Computers, 2000-2008.
19. *Associate Editor*,
    - IEEE Transactions on VLSI, 2000-2003.

- IEEE Transactions on Circuits and Systems I, 1999-2001.
- IEEE Transactions on Circuits and Systems II, 1999-2008.
- Journal of Circuits, Systems, and Computers, 1999-2000.
- Editor-at-Large, Marcel Dekker Inc., New York, Basel.

20. *Chair*, Plenary Sessions, 13th International Conference on Digital Signal Processing, July 12-14, 1997, Santorini, Greece.
21. *Technical Program Committee Member* of the Conferences/Symposia:
    - 2nd International Workshop on Signal and Image Processing, Nov. 8-10 1995, Budapest.
    - 1998 SCS/IEEE Symposium on Performance Evaluation of Computer and Telecommunication Systems (SPECTS'98), July 19-22, 1998, Reno, Nevada.
    - IEEE International Phoenix Conf. on Computers and Communications (IPCCC), Phoenix, AZ, 1996-.
    - Int. Conference on Application Specific Systems Architectures and Processors (ASAP), 1996-7.
    - Euromicro 97, Budapest, September 1997.
    - COMBIO '96, Sopron, Hungary, 1996.
    - IEEE Workshop on Design and Implementation of Signal Processing Systems (SiPS) 1997-00.
    - IEEE Grate Lakes Symposium on VLSI (GLS 98), Lafayette, LA, 19-21 Feb. 1998.
    - XIII Int. Conf. on Microelectronics and Packaging, Curitiba-Parana, BRAZIL, August 1998.
    - IEEE International Conference on Acoustics Speech and Signal Processing (ICASSP), Phoenix, AZ, 1999.
22. *Session Chair* of International Conferences/Symposia: (ICECS, COMBIO, MMA, MWSCAS, ISCAS, SiPS, PATMOS).
23. *Steering Committee Member,* IEEE ICECS.
24. *European Liaison* of IEEE Int. Phoenix Conf. on Computers and Communications, IPCCC'98.
25. *Reviewer* for IEEE Transactions on ASSP, C&S, VLSI, and Computer. Also for IEE Electronics Letters και IEE Proceedings E, F, and G, as well as for World Scientific, International Journal on Electronics, Systems, and Computers.
26. *Reviewer* for the IEEE Conferences: ICASSP, ISCAS, ICECS, and ASAP, VLSI 9*, EuroDAC.
27. *Proposal Reviewer*
    - USA National Science Foundation,
    - Joint NSF (USA)-GSRT (GREECE) funding,
    - British Engineering and Physical Sciences Research Council (EPSRC),
    - European Commission ESPRIT program.
28. *Award Committee member* for the IEEE Society of Circuits and Systems, 1997.
29. *Consultant*, VLSI Technology, California and The Athena Group, Florida, 1986.
30. *Faculty Advisor*, Hellenic Student Association of the Ohio State University, 1989-1990.
31. *Fellowship,* Greek State Scholarships Foundation, 1975-1976.
32. *Graduate Fellowship,* University of Cincinnati, 1981-1983 and University of Florida, 1983-1986.
33. *Outstanding Ph.D. Dissertation Award,* University of Florida, 1986.
34. *Certificate of Appreciation*, IEEE Society of Circuits and Systems, 1997-2013.
35. *Certificate of Appreciation*, IEEE Technical Activities Board, 2012-2013.

AFFILIATIONS

- Fellow of IEEE and member of its Computer, Circuits and Systems, and Signal Processing Societies.
- Member of Association for Computer Machinery

COMMERCIAL PRODUCT

- DF-PAK: an integrated software package for digital filter design on personal computers, 1985. (This is the first ever package designed for the IBM PC.)

PATENTS

- A *Hybrid Signed-Digit/Logarithmic Number System Processor, USA* patent number: 5097434; issued on March 17, 1992.
- Multiplication *of Complex Numbers Using Polynomial Models*, USA patent office application number: 282,307.
- Dual-field *Residue Arithmetic Montgomery Multiplier Methods and Apparatus,* submitted to WIPO, August 2012.

INVITED/KEYNOTE SPEECHES

1. *Logarithmic Number System Processors*, Invited Talk, University of Rhode Island, May 1987.
2. *High-Speed Digital Arithmetic Architectures*, Invited Talk, Drexel University, April 1987.
3. *RNS Processors: Problems and Perspectives*, Invited Talk, George Mason University, June 1987.
4. *Teaching Digital Signal Processing*, Invited Talk, Technical University of Sofia, June 1993.
5. *Computer Arithmetic and DSP Applications,* Invited Talk, University of Thrace, May 1997.
6. *The Impact of Arithmetic in Lowering the Chip Energy Consumption*, Plenary Talk, NORCHIP 2000, Turku, Finland Nov. 2000.
7. *Low-Power Video Processing,* Invited Talk, Columbia University, May 2002.
8. *Data Representation and Reuse in DSP Algorithms: An Ecological Dimession,* Plenary Talk, 2008 International SOC Design Conference, Nov. 2008, Busan, Korea
9. "*Low Power Data Representation in DSP algorithms*," Plenary Talk, 2009 CISP-BMEI International Conference, Oct. 2009, Tianjin, China.
10. "*Advances in Cryptography System Implementations*," Plenary Talk, 2011 CISP-BMEI International Conference, Oct. 2011, Shanghai, China.
11. *Cryptography Hardware Advances,"* Plenary Talk, 2012 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Dec. 2012, Kaohsiung, Taiwan.
12. «*Cryptographic System Implementations*»," Plenary Talk, The 17th CSI International Symposium on Computer Architecture & Digital Systems **(**CADS 2013), Oct. 29-31, 2013, Tehran, Iran.
13. «*Flexible Cryptographic Systems*»," The IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2014), Nov. 17-20, 2014, Ishigaki Island, Okinawa, Japan.

COURSES DEVELOPED AND/OR TAUGHT

1. Electric Circuits (two-semester course, University of Florida).
2. Basic Principles of Electrical Engineering (one-semester course, University of Florida).
3. Micro-processors (one-semester course, University of Florida).
4. Control Systems: a state-space approach (one-semester course, University of Florida).
5. Computer Architecture (one-semester course, Ohio State University).
6. Computer Arithmetic (one-semester course, Ohio State University).
7. Digital Design (one-semester course, Ohio State University).
8. Digital Signal Processing*** (two-semester course w/ lab, Ohio State University and Univ. of Patras).
9. Digital Image Processing (one-semester course, Univ. of Patras).
10. VLSI Design (one-semester course, New York University)
11. VLSI Signal Processing (one-semester course, Univ. of Patras, New York University, Univ. of British Columbia-directed studies).
12. Foundations of Computer Science - Discrete Mathematics (one-term course, ICICS, Univ. of British Columbia).

TUTORIAL COURSES OFFERED IN CONFERENCES

- "*Elliptic Curve Cryptography: Security, Hardware Implementation, Future Outlook*," 16th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2009, Hammamet, Tunisia, December 13, 2009 (Schinianakis, D., Stouraitis, T).
- "*Elliptic Curve Cryptography: Security, Hardware Implementation, Future Outlook*," IEEE International Symposium on Circuits and Systems, selected at ISCAS 2010, Paris, France, May 29, 2010 (Schinianakis, D., Stouraitis, T).
- "*Elliptic Curve Cryptography: Computer Arithmetic, Hardware Implementation, Future Outlook*," 18th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2011, Beirut, Lebanon, December 2011 (Schinianakis, D., Stouraitis, T).

FUNDED RESEARCH PROGRAMS

1. Principal Investigator, *"Multiprocessor Architectures for Hybrid Logarithmic Number System Units",* $17 700, OSU Seed Grant, April 1988 - September 1989.
2. Researcher, *Esprit Basic Research Action 3281, ASCIS,* 1989-1991.
3. Principal Investigator, *"Parallelization of Automatic Control Algorithms and their VLSI Implementation",* Greek Secretariat of Research and Technology, ECU 40 000, September 92 - August 94.
4. Principal Investigator, *"Fault Detection for Textile Industry using Computer Vision",* STRIDE HELLAS, (LIGHT), Greek Secretariat of Research and Technology, ECU 50 000, 1992-3.
5. Principal Investigator, *"Advanced Digital Signal Processing Course",* European Commission Funds, ECU 45 000, 1992-3.
6. Principal Investigator, *"HEAR: A General Hearing-Aid Processor",* ESPRIT Project 8560, ECU 760 000, 1993-1996.
7. Principal Investigator, *"Texture Analysis: Advanced Methods and Applications",* A PHARE-ACCORD Project, ECU 40 000, 1993-1995.
8. Researcher, *"Vision Algorithms and Optical Computer Architectures",* HCM Project, ECU 130 000, 1993-1995.
9. Principal Investigator, *"Optimal Arithmetic Processors for Multimedia Applications",* PENED95 494, Greek Secretariat of Research and Technology, ECU 30 000, May 96 - April 98.
10. Principal Investigator, "Assessment *of Change in the Appearance of Fabrics Using Computational Image Processing Methodology",* (FABRICIMAGE), Phare TDQM HV-9305-02. 40.000 ECU, 1996-8.
11. Researcher, "Human *Network for the use and Distribution of Advanced Communication media for the Collaboration of Research and Development* Units," EPEAEK 95, 40.000 ECU, 1996-8.
12. Researcher, "Human *Network for: Artificial Neural Networks-Prospects and Applications,"* EPEAEK 95, 40.000 ECU, 1996-8.
13. Principal Investigator, "Low-Power *Software Development for Embedded Applications,"* (SOFLOPO), ESPRIT ESD Pilot Action for Low-Power Design, Project 25403, 576.000 ECU, Nov. 1997-9.
14. Director, "*International Multidisciplinary Graduate Program on Signal and Image Processing: Theory, Implementations, Applications*", Greek Ministry of Education, Euro 370.000, 1997-2004.
15. Principal Investigator, "Experimental ADSL Network *for Fast Internet and Multimedia Services," OTE, Euro* 40.000, 1998-1999.
16. Researcher, "Unification of *Wireless Access Using DECT Technology in Existing and Future OTE Systems/Networks*," OTE, Euro 75.000, 1998-1999.
17. Principal Investigator, "Advanced *DSP Techniques for Telecommunications Applications,"* Euro 100.000, Greek Secretariat of Research and Technology, 1999-2002.
18. Principal Investigator, *"Wavelet-based video coding for dynamic-transmission environments,"* Euro 66.924, Interuniversitair Micro-Elektronica Centrum vzw IMEC, 2003-2006.
19. Research Group Leader, *"Advanced DSP Systems for Wide-band Communications and Video,"* Euro 170.000, ΕΚΤ-ΕΠΕΑΕΚ ΙΙ-ΠΥΘΑΓΟΡΑΣ ΙΙ, 2005-7.

20. Principal Investigator, "*Advanced Cryptography System Architectures*," Euro 45.000, Heraklitos Program Greek Government, 2011-2013.
    Research Collaborator*, "Cognitive Platform for Ubiquitous Cloud-based Gaming,"* CAD 495.000, NSERC Canada, 2014-16.

Total Funding: (Approx. Euro 2.650.000)

PUBLICATIONS

Ph.D. Thesis: *Logarithmic Number System Theory, Analysis and Design,* University of Florida, Gainesville, Florida, 1986. It won the 1986 Outstanding Dissertation Award.

Master's Thesis: *Design and Construction of a MODEM,* University of Athens, Athens, Greece, 1981.

Books:

- Digital *Filter Design Software for the IBM-PC, Marcel* Dekker Inc., New York, 1987 (F. Taylor, T. Stouraitis).
- Digital *Signal Processing, University* of Patras Press, 1997 (T. Stouraitis).
- Advanced *Signal Processing, Circuits, and System Design Techniques for Communications*, IEEE 2006 (Paliouras, V., Stouraitis, T., Ioinovici, A., eds.).

Book Chapters:

1. *"Complex Multiplication Using the Polynomial Residue Number System",* in **Advances in Computing and Controls**, edited by W. A. Porter, S. C. Kak, and J. L. Aravena, Springer-Verlag, pp. 61-70, 1989 (with A. Skavantzos).
2. *"On the Design of Two-Level Pipelined Processor Arrays",* in **Application-Driven Synthesis Methodologies for Real-Time** Processor Architectures, eds. F. Catthoor, L. Svensson and K. Wolcken, Kluwer Academic Publishers, 1993 (with D. Soudris, E. Kyriakis-Bitzaros, M. Birbas, V. Paliouras and C. Goutis).
3. *"A Neural Methodology for Mapping Nested-Loop Algorithms to Heterogeneous Processor Arrays***", in Recent Advances in Circuits** and Systems, World Scientific Publishing Co., pp. 323-336, 1998. (K. Karagianni, A. Tzigkounakis, C. Goutis and T. Stouraitis).
4. "Computer Arithmetic Techniques for Low-Power Systems", in **Designing CMOS Circuits for Low Power**, edited by Dimitrios Soudris, Christian Piguet, and Costas Goutis, Kluwer Academic Publishers, pp. 97-115, 2002. (V. Paliouras, T. Stouraitis).
5. *"Low-Energy Software Optimization for the ARM7* Processor: The Software Scheduling Approach", in **System-Level Power Optimization for Wireless Multimedia Communication** (Power-aware computing), edited by Ramesh Karri, and David Goodman, Kluwer Academic Publishers, pp. 87-96, 2002. (G. Synevriotis, T. Stouraitis).
6. "Logarithmic *and Residue Number Systems for VLSI Arithmetic", in Electrical Engineer's* Handbook, **Academic Press, pp. 179-190, 2004.** (T. Stouraitis).
7. "Residue number systems in cryptography: design, challenges, cryptanalysis," in **Secure System Design and Trustable Computing***,* edited by Chip-Hong Chang and Miodrag Potkonjak, Springer International Publishing AG, Switzerland, in print, (D. Schinianakis and T. Stouraitis).

Journal Papers:

1. "A Radix-4 FFT Using Complex RNS Arithmetic," *IEEE Transactions on Computers,* Vol. C-34, no. 6, pp. 573-576, June 1985 (F. Taylor, G. Papadourakis, A. Skavantzos, and T. Stouraitis). The paper is included in the 1986 *IEEE Press publication on Residue Arithmetic.*
2. "DF-PAK: A Digital Filter Design Software Package,*" IEEE Transactions on* Education, vol. E-31, no. 1, pp. 34-38, February 1988 (T. Stouraitis, F. Taylor).
3. "Analysis of Logarithmic Number System Processors," *IEEE Transactions on Circuits and Systems,* vol. CAS-35, no. 5, pp. 519-527, May 1988 (T. Stouraitis, F. Taylor).
4. "Floating-Point to Logarithmic Encoder Error Analysis,' IEEE Transactions on Computers, vol. C-37, no. 7, pp. 858-863, July 1988 (T. Stouraitis, F. Taylor).
5. "Decomposition Of Complex Multipliers Using Polynomial Encoding," IEEE Transactions on Computers , vol. C-41, no. 10, pp. 1331-1333, October 1992 (A. Skavantzos, T. Stouraitis).
6. "Complex Multiplication using the Polynomial Residue Number system," chapter in book *Advances in Computers and Controls,* edited by W. A. Porter, S. C. Kak, J. L. Aravena, Spinger-Verlag, pp. 61-70, 1989 (A. Skavantzos, T. Stouraitis).
7. "Multiplication of Complex Numbers Encoded as polynomials," *Journal of VLSI Signal Processing,* Special Issue on Computer Arithmetic, vol. 3, pp. 319-328, 1991 (T. Stouraitis, A. Skavantzos).
8. "Fast Digit-Parallel Conversion of Signed-Digit Into Conventional Representations," vol. 27, no. 11, pp. 964-965, *IEE Electronics Letters* (C. Chen, T. Stouraitis).
9. "Efficient Converters for Residue and Quadratic Residue Number Systems," *IEE Proceedings-G,* vol. 139, no. 6, pp. 626-634, 1992 (T. Stouraitis).
10. "Full Adder-Based Arithmetic Units for Finite Integer Rings," *IEEE Transactions on Circuits and Systems,* vol. 40, no. 11, November 1993, (T. Stouraitis, S. Kim , A. Skavantzos).
11. "Analogue-and Binary-to-Residue Conversion Schemes," *IEE Proceedings-G: Circuits, Devices and Systems,* vol. 141, No. 2, pp. 135-139, April 1994 (T. Stouraitis).
12. "Borrow: A Fault-Tolerance Scheme For Wavefront Array Processors," IEEE Transactions on Computers, vol. 42, no. 10, pp. 1257-1261, October 1993 (T. Stouraitis).
13. "Performance Evaluation of BIN/ABIN Networks in Buffered/Unbuffered Packet-Switched Environments," *IEE Proceedings-E*, vol. 141, no. 1, pp. 29-34, Jan. 94 (T. Stouraitis).
14. "Hybrid Signed-Digit/Logarithmic Number System Processor," IEE *Proceedings-E, vol*. 140, no. 4, pp. 205-210, 1993 (C. Chen, and T. Stouraitis).
15. "Polynomial Residue Complex Signal Processing," *IEEE Transactions on Circuits and Systems*, vol. 40, no. 5, pp. 342-344, 1993 (A. Skavantzos, T. Stouraitis).
16. "Prime-Factor DCT Algorithms," IEEE Transactions *on Signal Processing vol. 43, no*. 3, pp. 772-776, March 1995 (A. T. Tatsaki, C. Dre, T. Stouraitis, and C. Goutis).
17. "Image Coder based on *Residue Number System for Progressive* Transmission," IEE Electronics Letters, vol. 41, no. 6, pp. 442-443 (A. T. Tatsaki, T. Stouraitis, and C. Goutis).
18. "On the Computation of the prime factor 1-D discrete sine transform,*" Signal Processing,* North-Holland Elsevier, vol. 42, no. 3, pp. 231-236, 1995 (A. T. Tatsaki, C. Dre, T. Stouraitis and C. Goutis).
19. "A VLSI Design Methodology for RNS Full Adder-Based Inner Product Architectures," *IEEE Transactions* on Circuits and Systems - Part II, April 1997, vol. 44, no. 4, pp. 315-318 (V. Paliouras, D. Soudris, T. Stouraitis, and C. Goutis).
20. "Trade-Off Analysis of a Low-Power Image Coding Algorithm," Journal of VLSI *Signal Processing Systems for Signal, Image and Video Technology*, vol. 18, pp. 65-80, 1998, special issue on Systematic Trade-Off Analysis in Signal Processing Systems Design (K. Masselos, P. Merakos, T. Stouraitis, and C. E. Goutis).
21. "A Novel Algorithm for Low-Power Image and Video Coding,*" IEEE Transactions on Circuits and Systems for Video Technology, vol. 8,* no. 3, June 1998, pp.258-263 (K. Masselos, P. Merakos, T. Stouraitis, and C. E. Goutis).

22. "Efficient Processor Arrays for the Implementation of the Generalized Predictive Control Algorithm," *IEE Proceedings D- Control Theory and Applications*, vol. 145, no. 1, January 1998 (K. Karagianni, Th. Chronopoulos, A. Tzes, N. Kousoulas, and T. Stouraitis).
23. "Design Methodology for the implementation of multidimensional Circular Convolution," *IEE Proceedings-Circuits, Devices, and Systems, vol. 144, no*. 6, December 1997, (D.J. Soudris, V. R. Paliouras, T. Stouraitis, and A. Thanailakis).
24. "Novel Scheme for Low-Power Classified Vector Quantization Image Coding," IEE proceedings on Vision, Image and Signal Processing, Vol. 145, No. 6, December 1998, pp. 408-414, (K. Masselos, T. Stouraitis, C. E. Goutis).
25. "Novel Vector Quantization Based Algorithms for Low Power Image Coding and Decoding," *IEEE Transactions on Circuits and Systems II,* Vol. 46, No. 2, pp. 193-198, February 1999 (K. Masselos, P. Merakos, T. Stouraitis, C. E. Goutis).
26. "Error Bounds for Floating-Point Polynomial Interpolators," IEE Electronics Letters, Vol*. 35, No. 3, pp. 195-197,* 4th February 1999 (V. Paliouras, K. Karagianni, T. Stouraitis).
27. "Novel Techniques for Bus Power Consumption Reduction in Realizations of Sum-of-Product Computation", *IEEE Transactions on VLSI Systems,* 7: (4) 492-497 Dec 1999 (K. Masselos, P. Merakos, T. Stouraitis, C. E. Goutis).
28. "Computation Reordering: A Novel Transformation for Low Power DSP Synthesis," VLSI Design Journal, Gordon and Breach Science Publishers SA, 10: (2) 177-202, 2000 (K. Masselos, P. Merakos, T. Stouraitis, C. E. Goutis).
29. "Multi-Function Architectures for RNS Processors," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, August 1999, vol. 46, no. 8, pp. 1041-1054 (V. Paliouras, T. Stouraitis). Awarded the 2000 IEEE Circuits and Systems Society **Guillemin-Cauer *Award.*** The abstract of this article has also been included in the *IEEE Circuits and Systems Society Newsletter*, Vol. 11, No. 2, pp. 29, June 2000.
30. "Low Power Architectures for Digital Signal Processing," Journal of Systems Architecture, Elsevier Publishers**,** *46: (7) 551-571 Apr. 15 2000* (K. Masselos, P. Merakos, T. Stouraitis, C. E. Goutis).
31. "A floating-point processor for fast and accurate sine/cosine evaluation," IEEE Transactions *on Circuits and Systems II,* Vol. 47, No. 5, pp. 441 – 451, May 2000. (V. Paliouras, K. Karagianni, T. Stouraitis)
32. "Novel High-Radix Residue Number System Processors," IEEE Transactions on Circuits and *Systems – Part* II, Vol. 47, No. 10, pp. 1059-1073, October 2000 (V. Paliouras and T. Stouraitis)
33. "Operation Saving VLSI Architectures for 3-D Geometrical Transformations," *IEEE Transactions on Computers,* vol. 50, no. 6, pp. 609 -622, June 2001 (K. Karagianni, V. Paliouras, G. Diamantakos, T. Stouraitis).
34. "Considering the Alternatives in Low-Power Design," IEEE *Circuits and* Devices Magazine, pp. 23-29, July 2001 (T. Stouraitis and V. Paliouras).
35. "A Low-Complexity Combinatorial RNS Multiplier," IEEE Transactions on Circuits and *Systems* - Part *II, vol. 48, no. 7, pp*. 675-683, July 2001 (V. Paliouras, K. Karagianni, and *T. Stouraitis).*
36. *"A* Systolic Array Architecture for the Discrete Sine Transform," IEEE Transactions *on Signal Processing*, vol. 50, no. 9, pp. 2347-2354, September 2002 (D. F. Chiper, M.N.S. Swamy, M.O. Ahmad, and T. Stouraitis). **This paper, together with J41, received the Romanian Academy prize for 2005.**
37. "Memory Accesses Reordering for Interconnect Power Reduction in Sum-of-Products Computations," IEEE Transactions on *Signal Processing, vol. 50, No.* 11, pp. 2889-2899, November 2002. (K. Masselos, S. Theoharis, P. Merakos, T. Stouraitis, C. E. Goutis).
38. "Optimization Techniques for Reducing Global Bus Switching Activity in Realizations of *Sum-of-Products Computations in DSP Systems", IEE* Proceedings on Circuits Systems and Devices , vol. 150, No. 1, pp. 16-26, February 2003. (P. Merakos, K. Masselos, S. Theoharis, T. Stouraitis, and C. E. Goutis).
39. "New Power-of-2 RNS Scaling Scheme for Cell-Based IC Design", IEEE Transactions on *VLSI Systems, vol. 11, no*. 2, pp. 1-5, April 2003 (Uwe Meyer-Baese and T. Stouraitis).

40. "Power Efficient Data Path Synthesis of Sum-of-Products Computations," *IEEE Transactions on Very Large Scale of Integration (VLSI) Systems,* vol. 11, no. 3, pp. 446-450, June 2003 (K. Masselos, P. Merakos, S. Theoharis, T. Stouraitis, and C. E. Goutis).
41. "Systolic Algorithms and *a Memory-Based* Design *Approach for a Unified Architecture for the Computation of* DCT/DST/IDCT/IDST," IEEE Transactions on Circuits and Systems-II, vol. 52, *no. 6, pp. 1125-1137, June 2005 (D*. F. Chiper, M.N.S. Swamy, M.O. Ahmad, and T. Stouraitis). **This paper, together with J36, received the Romanian Academy prize for 2005.**
42. *"Hidden* Messages in Heavy-Tails: DCT-Domain Watermark Detection Using Alpha-Stable *Models,"* IEEE Trans. on Multimedia, vol. 7, No. 4, pp. 700-715, August 2005. (Alexia Briassouli, Panagiotis Tsakalides and Athanasios Stouraitis).
43. "Performance Comparison of Two-dimensional Discrete Wavelet Transform Computation *Schedules on a VLIW Digital Signal* Processor," IEE Proceedings Vision, Image & Signal Processing, vol. 153, issue 2, pp. 173 – 180, 6 April 2006 (Konstantinos Masselos, Yiannis Andreopoulos and Thanos Stouraitis).
44. "Optimized Memory Requirements for Wavelet-Based *Scalable Multimedia Codecs," Journal of Embedded Computing, vol. 1, issue 3 (August* 2005), pp: 363-380 (V. Ferentinos, G. Lafruit, M. Milia, J. Bormans, F. Catthoor, and T. Stouraitis**).**
45. Large Dynamic Range RNS Systems and Their Residue to Binary Decoders," *Journal of Circuits and Systems and Computers***,** vol. 16, no. 2, pp. 267 – 286, April 2007 (A. Skavantzos, M. Abdallah, and T. Stouraitis).
46. "An RNS Implementation of an FP Elliptic Curve Point Multiplier," *IEEE Transactions on Circuits and* Systems-II, vol. 56, no. 6, June 2009 (D. Schinianakis, A.P. Fournaris, H.E. Michail, A.P. Kakarountas, and T. Stouraitis).
47. "Exploiting varying resource *requirements in* wavelet-based *applications in dynamic execution environments," Journal of* Signal Processing Systems, vol. 56, pp. 125 – 139, March 2009 (B*. Geelen, V. Ferentinos, F*. Catthoor, S. Toulatos, G. Lafruit, T. Stouraitis, R. Lauwereins, D. Verkest).
48. "Spatial locality exploitation for runtime reordering of JPEG2000 wavelet data layouts," *ACM Transaction on Design Automation of Electronic Systems* (TODAES), 15(1): (2009) Article No.: 8 DOI: 10.1145/1640457.1640465, (B. Geelen, V. Ferentinos, F. Catthoor, G. Lafruit, D. Verkest, R. Lauwereins, and T. Stouraitis).
49. "Modeling and Exploiting Spatial Locality Trade-Offs in Wavelet-Based Applications under Varying Resource Requirements," *ACM Transactions on Embedded Computing Systems,* vol. 9, no. 3, Article 17, February 2010. DOI: 10.1145/1698772.1698775 (B. Geelen, V. Ferentinos, F. Catthoor, G. Lafruit, D. Verkest, R. Lauwereins, T. Stouraitis).
50. "Efficient RNS Implementation of Elliptic Curve Point Multiplication Over GF(p)," I*EEE Transactions on Very Large Scale Integration Systems*, Jan. 2012 (M. Esmaeildoust, D. Schinianakis, H. Javashi, T. Stouraitis, and K. Navi).
51. "Multifunction Residue Architectures for Cryptography," *IEEE Transactions on Circuits and Systems* I, vol. 61, no. 4, pp. 1156 – 1169, April 2014. DOI: 10.1109/TCSI.2013.2283674 (Schinianakis, D. and T. Stouraitis).
52. "An Orthogonal Wavelet Division Multiple-Access Processor Architecture for LTE-Advanced Wireless/Radio-over-Fiber Systems over Heterogeneous Networks," *EURASIP Journal on Advances in Signal Processing* 2014:77 doi:10.1186/1687-6180-2014-77 (Chinmaya Mahapatra, Victor C.M. Leung and Thanos Stouraitis).
53. "Area-Throughput Trade-offs for SHA-1 and SHA-256 Hash Functions' Pipelined Designs," accepted for publication in *Journal of Circuits, Systems and Computers* (H.E. Michail, G.S. Athanasiou, G. Theodoridis, T. Stouraitis, and C.E. Goutis).
54. "A High Speed FPGA Implementation of an RSD Based ECC Processor," *IEEE Transactions on Very Large Scale Integration Systems*, accepted for publication in 2015 (H. Marzouqi, M. Al-Qutayri, K. Salah, D. Schinianakis, and T. Stouraitis).

Journal Issue:

55. *ACM/Springer Mobile Networks and Applications (MONET)*: "SM 148 - QSHINE 2014" - Half Special Issue on "Quality of Service in Heterogeneous Wireless Networks," Guest Editors: Edith C.-H. Ngai, Victor C.M. Leung, Jiangchuan Liu, Jianping Pan, and T. Stouraitis.

Conference Papers:

1. "A Reconfigurable Systolic Primitive Processor for Signal Processing," *Proceedings of IEEE International Conference on Acoustics, Speech, and Signal Processing*, Tampa, FL, March 1985, pp. 8.10 (T. Stouraitis, S. Natarajan and F. Taylor).
2. "An Adaptive Radix Reconfigurable Processor for Signal Processing," *Proceedings of the IASTED International Symposium,* pp. 333-336, Paris, June 19-21, 1985 (T. Stouraitis, F. Taylor, G. Papadourakis, and A. Skavantzos).
3. "Logarithmic Kalman Filter," *Proceedings of the IASTED International Symposium*, pp. 48-51, Paris, June 19-21, 1985 (G. Papadourakis, T. Stouraitis, and A. Skavantzos).
4. "Computing DFT's Digital Convolution and Correlation Using Complex RNS Arithmetic," *Proceedings of the IASTED International Symposium,* pp. 277-280, Paris, June 19-21, 1985 (A. Skavantzos, T. Stouraitis, and G. Papadourakis).
5. "Residue Complex Multipliers," *Proceedings of the 26th Annual Allerton Conference on Communication, Control and Computing,* Allerton House, Monticello, Illinois, September 28-30, 1988 (A. Skavantzos, T. Stouraitis,).
6. "Complex Multiplication Using the Polynomial Residue Number System," *Proceedings of the 1988 COM CON,* Baton Rouge, LA, October 19-21, 1988.
7. "Parallel Decomposition of Complex Multipliers," *Proceedings of the 22nd Annual Asilomar Conference*, Pacific Grove, California, October 31-November 2, 1988 (T. Stouraitis, A. Skavantzos).
8. "A Complex DSP Processor Using Polynomial Encoding," *Proceedings of the 1989 IEEE International Conference on Acoustics, Speech, and Signal Processing,* Glasgow, Scotland, May 23-26, 1989 (A. Skavantzos, Z. Sarkari, T. Stouraitis).
9. "An Efficient VLSI Implementation of Logarithmic Signal Processors," *Proceedings of the 1989 International Symposium on Circuits & Systems,* Portland, Oregon, May 9-11, 1989 (T. Stouraitis).
10. "A Hybrid Floating-Point/Logarithmic Number System Digital Signal Processor," *Proceedings of the 1989 International Conference on Acoustics, Speech and Signal Processing,* Glasgow, Scotland, May 23-26, 1989 (T. Stouraitis).
11. "A Reconfigurable Systolic Array for Polynomial Multiplication Modulo $X^n \pm 1$," *Proceedings of the IEEE 21st Southeastern Symposium on System Theory (SSST-89),* Tallahassee, Florida, March 26-28, 1989 (Z. Sarkari, A. Skavantzos, T. Stouraitis).
12. "Dual-Mode VLSI Array for Polynomial Multiplication Using Residue Arithmetic," *Proceedings of the IEEE 1989 Southeastcon,* Columbia, South Carolina, April 9-12, 1989 (Z. Sarkari, A. Skavantzos, T. Stouraitis).
13. "Processor-Memory Interconnection Issues for Multiprocessor Systems," *Proceedings of the 23rd Annual Asilomar Conference,* Monterey, California, October 1989 (H.P. Chan, T. Stouraitis).
14. "Efficient Analog-to-RNS Conversion Schemes," *Proceedings of the 1990 International Symposium on Circuits & Systems,* N. Orleans, LA, 1990 (S. Mandyam, T. Stouraitis).
15. "Implementing Complex Multipliers by Means of Polynomial Products," *Proceedings of the 24th Annual Asilomar Conference,* Monterey, California, November 1990 (A. Skavantzos, T. Stouraitis).
16. "New Implementations of Converters for the Residue and the Quadratic Residue Number Systems," *Proceedings of the 1991 IEEE International Symposium of Circuits and Systems,* Singapore, May 1991 (S. Kim, T. Stouraitis).
17. "Parallel Implementations of Inner Product Step Processors," *Proceedings of the ISMM International Workshop on Parallel Computing,* pp. 32-35, Trani, Italy, September 10-13, 1991 (T. Stouraitis, A. Skodras).

18. "Systematic Development of Architectures for Multidimensional DSP Using the Residue Number System," *Proceedings of the 1992 IEEE International Conference on Acoustics, Speech, and Signal Processing*, March 23-26, 1992, San Francisco, USA (D. Soudris, V. Paliouras, T. Stouraitis).
19. "Systematic Derivation of the Processing Element of a Systolic Array Based on the Residue Number System," *Proceedings of the 1992 International Symposium on Circuits and Systems,* San Diego, California, May 10-13, 1992 (V. Paliouras, D. Soudris, T. Stouraitis).
20. "Systematic Design of Full-Adder Based Architectures for Convolution," *Proceedings of the 1993 IEEE International Conference on Acoustics, Speech, and Signal Processing*, pp. I.389-I.392, April 1993, Minneapolis, USA, (D. Soudris, V. Paliouras, T. Stouraitis, A. Skavantzos and C. Goutis).
21. "Methodology for the Design of Signed-Digit DSP Processors," *Proceedings of the 1993 International Symposium on Circuits and Systems, ISCAS '93,* May 3-6, 1992, Chicago, IL, USA (V. Paliouras, D. Soudris, T. Stouraitis).
22. "Full-Adder Based Inner Product Step Processors for Residue and Quadratic Residue Number Systems," *Proceedings of the 1993 International Symposium on Circuits and Systems, ISCAS '93,* May 3-6, 1992, Chicago, IL, USA (S. Kim, T. Stouraitis, A. Skavantzos).
23. "A Fast Cosine Pruning Algorithm," *Proceedings of the International Conference on Digital Signal Processing and Computer Applications to Engineering Systems (ICCAES)*, Cyprus, July 14-16, 1993 (A. Skodras, K.M. Curtis, T. Stouraitis, N.P. Walmley).
24. 'A Novel Prime-Factor Algorithm for the 1-D and 2-D Discrete Cosine Transform," *Proceedings of the 1993 European Conference on Circuit Theory and Design*, Davos, Switzerland, 1993 (Ch. Dre, A. Tatsaki, T. Stouraitis, and C. Goutis).
25. "Efficient Texture Analysis Implementations," *Phare-Accord Texture Workshop*, Patras, December 1993 (G. Karayiannis, T. Stouraitis).
26. "A Novel Prime Factor Algorithm for the 1-*D* and the 2-*D* Discrete Cosine Transform," *Proceedings of the 1993 European Conference on Circuit Theory and Design* (ECCTD'93), pp. 797-802, Davos, 1993 (with C. Dre, A. T. Tatsaki, T. Stouraitis, and C.E. Goutis).
27. "Systematic Design of Multi-Modulus/Multi-Function Residue Number System Processors," *IEEE International Symposium on Circuits and Systems* (ISCAS `94), May 30-June 2 1994, London, pp. 4.79-4.82 (V. Paliouras, T. Stouraitis).
28. "An Efficient Pyramid VQ-based Image Compression Algorithm," *IEEE Data Compression Conference* (DCC'94), pp. 479, Snowbird, Utah, March 1994. (A. Tatsaki, T. Stouraitis, C. Goutis).
29. "Mapping Iterative Algorithms onto Processor Arrays by the Use of Petri Net Models," *IEEE First International conference on Massively Parallel Computing Systems*, pp. 140-151, May 2-6, 1994, Ischia, Italy, (K.E. Karagianni, E.D. Kyriakis-Bitzaros, T. Stouraitis).
30. "Modelling of Algorithms and Processor Arrays Based on Cellular Automata," *7th International Conference on Modelling Techniques and Tools for Computer Performance Evaluation*, pp. 63-66, May 4-6, 1994, Vienna (V. Paliouras, E.D. Kyriakis-Bitzaros, T. Stouraitis, and C.E. Goutis).
31. "Non-Linear Optimization: Artificial Neural Network Solution Techniques Applied to the Optimum Linear Feedback Control of Linear Discrete-Time Dynamic Systems," *20th Euromicro Conference: System Architecture and Integration*, Liverpool, U.K., October 1994 (G.-P. K. Economou, P.K. Anagnostopoulos, G.C. Theofilou, T. Stouraitis, and C.E. Goutis).
32. "Texture Classification by Measuring the Fractal Dimension Vector in a Wavelet Decomposed Image," *Proc. of 8th Symposium on Microcomputer and Microprocessor Applications*, Budapest, Hungary, October 1994 (with Y.A. Karayiannis, T. Stouraitis, G.-P. K. Economou, and N.M. Economopoulos).
33. "Multi-operational Logarithmic Number System Adders and Subtractors based on Polynomial Approximation" *ICECS '94*, pp. 250-253, Cairo, December 1994 (V. Paliouras, I. Orginos, T. Stouraitis).
34. "Progressive Image Compression Algorithm Based on Lattice Vector Quantization*", EUROPTO: The European Symposium on Advanced Networks and Services in Compression Technologies and Standards for Image and Video Communications*, RAI, Amsterdam, March 1995 (A. T. Tatsaki, T. Stouraitis, and C. Goutis).

35. "An Efficient Address-Vector-Quantization-Based Image Coding Scheme," *SPIE Advanced Network Services: Compression Technologies and Standards for Image and Video Communications*, Amsterdam, 20-23 March 1995 (C. Dre, T. Stouraitis, and C. Goutis).
36. "Alternative Architectures for the 2-D DCT Algorithm," *IEEE Int. Symposium on Circuits and Systems* (ISCAS '95), pp. 2156-2159, Seattle, May 1995 (C. Dre, A. T. Tatsaki, T. Stouraitis, and C. Goutis).
37. "A Novel Algorithm for Multi-operand Logarithmic Number System Addition and Subtraction Using Polynomial Approximation," *ISCAS '95*, Seattle, May 1995, (I. Orginos, V. Paliouras, T. Stouraitis).
38. "Texture Classification Using the Fractal Dimension as Computed in a Wavelet Decomposed Image," *1995 IEEE Workshop on Nonlinear Signal and Image Processing*, pp. 186-189, Neos Marmaras, 20-22 June 1995 (Y. Karayiannis, T. Stouraitis).
39. "Image Compression Using Fractal Coding and Vector Quantization," *1995 IEEE Workshop on Nonlinear Signal and Image Processing*, pp. 210-213, Neos Marmaras 20-22 June 1995 (Y.A. Karayiannis, K. Masselos, T. Stouraitis).
40. "A computationally efficient algorithm for adaptive image compression," *IEE International Conference on Image Processing and its Applications*, pp. 50-54, July 1995 (A. T. Tatsaki, T. Stouraitis, and C. Goutis).
41. "Wavelet-Transform based Image Coder," *IEE International Conference on Image Processing and its Applications*, July 1995 (C. Dre, T. Stouraitis, and C.E. Goutis).
42. "Chinese Remainder Theorem-Based Algorithm for Convolution," *DSP '95*, Cyprus, July 1995 (C. Dre, G. Lafruit, T. Stouraitis, J. Cornelis and C. Goutis)
43. "Optical Computers, System Aspects, Architectures and Simulator Environment," *DSP '95*, Cyprus, July 1995 (N. Langloh, H. Sahli, A. Kirk, V. Christopoulos, S. Van Langendock, A. Damianakis, F. Catthoor, T. Stouraitis, S. Orphanoudakis and J. Cornelis).
44. "Designing Efficient Redundant Arithmetic Processors for DSP Applications," *38th IEEE Midwest Symposium on Circuits and Systems*, pp. 1272-1275, Rio, Brazil, August 1995 (V. Paliouras, D. Soudris, T. Stouraitis).
45. "Systematic Design of Novel Architectures for Implementation of Radon Transform," *38th IEEE Midwest Symposium on Circuits and Systems, Rio*, pp. 1276-1279, Brazil, August 1995 (D. Soudris, T. Chronopoulos, N. Kousoulas, T. Stouraitis).
46. "A Petri Net Approach to the Design of Processor Array Architectures," *38th IEEE Midwest Symposium on Circuits and Systems*, pp. 37-40, Rio, Brazil, August 1995 (K.E. Karagianni, D. J. Soudris, T. Stouraitis).
47. "A Full-Custom Implementation of an RNS Multiplier," *ICECS '95*, pp. 25-28, Amman, Jordan, December 17-21, 1995 (A.R. Rjoub, V. Paliouras, T. Stouraitis).
48. "A Novel Algorithm for Accurate Logarithmic Number System Subtraction." *IEEE Int. Symposium on Circuits and Systems* (ISCAS '96), vol. 4, pp. 268-271**,** Atlanta, May 1996 (V. Paliouras, T. Stouraitis).
49. "Efficient Implementation of the Generalized Predictive Control Algorithm," *4th Mediterranean Symposium on New Directions in Control and Automation*, June 10-13 1996, Maleme, Crete, Greece, pp. 534-539 (K.E. Karagianni, Th. Chronopoulos, A. Tzes, N. Kousoulas, T. Stouraitis).
50. "Coding Wavelet Coefficients of Images," *Proceedings of the Third IEEE International Conference on Electronics, Circuits, and Systems (ICECS 96),* pp. 37-40, Rodos, Greece, October 13-16 1996 (C. Dre, T. Stouraitis).
51. "A Parallel Image Compression Scheme Based on Fractal Coding and Vector Quantization," *Proceedings of the Third IEEE International Conference on Electronics, Circuits, and Systems (ICECS 96),* pp. 712-715, Rodos, Greece, October 13-16 1996 (Masselos K., Karagianni K., Karayiannis Y.A., Stouraitis T.)
52. "Low-Power Image Decoding Using Fractals," *Proceedings of the Third IEEE International Conference on Electronics, Circuits, and Systems (ICECS 96),* pp. 748-751, Rodos, Greece, October 13-16 1996 (K. Masselos, P. Merakos, T. Stouraitis, and C. E. Goutis).
53. "Efficient Algorithms and VLSI Architectures for Trigonometric Functions in the Logarithmic Number System Based on the Subtraction Function," *Proceedings of the Third IEEE International Conference on Electronics, Circuits and Systems*, (ICECS`96), pp. 964-967, Rodos, Greece, October 13-16, (E. Malamas, V. Paliouras, T. Stouraitis).

54. "Architectural Optimization for a VLSI Digital Hearing-Aid Processor," *COMBIO`96*, Summer workshop on Computational Modelling, imaging and visualization in Biosciences, August 29-31 1996, Sopron, Hungary, pp. 99-103 (V. Paliouras, T. Stouraitis).
55. "An Operation-Saving VLSI Geometry Engine Core," *Proceedings of the 1997 IEEE International Conference on Acoustics, Speech, and Signal Processing*, Munich, Germany, vol. 1, pp. 607-610, April 1997 (K. Karagianni, G. Diamantakos, V. Paliouras and T. Stouraitis).
56. "Novel Codebook Design Techniques for Vector Quantization Image Compression," *1997 IEEE Int. Symposium on Circuits and Systems* (ISCAS '97) Hong Kong, June 1997 (K. Masselos, P. Merakos, T. Stouraitis, and C. E. Goutis).
57. "An Efficient Low-Power Bus Architecture," 1997 IEEE Int. Symposium on Circuits and Systems (ISCAS '97), Hong Kong, June 1997 (A. Rjoub, S. Nikolaidis, and O. Koufopavlou).
58. "Computationally Efficient Gradient Search Block Matching Algorithm for the Motion Estimation of Image Sequences," *Proceedings of the 13th International Conference on Digital Signal Processing (DSP 97),* pp. 797-800, Santorini, Greece, July 2-4 1997 (G. Sinevriotis and T. Stouraitis).
59. "Image Coding Using a Fractal/Vector Quantization Model," *Proceedings of the 13th International Conference on Digital Signal Processing (DSP 97),* pp. 797-800, Santorini, Greece, July 2-4 1997 (Masselos K., Kittes G., Karayiannis Y.A., Stouraitis T).
60. "Area-Time Performance of VLSI FIR Filter Architectures based on Residue Arithmetic," *Euromicro`97*, 1-4 September 1997, Budapest (V. Paliouras, T. Stouraitis).
61. "Design of Multimode Architectures," *Fourth International Conference on Electronics, Circuits, and Systems*, (ICECS 97), Cairo, Egypt, December 15-18 1997 (K.E. Karagianni T. Stouraitis).
62. "Image Coding Using Vector Quantization and a Logarithmic-Search Fractal Coding Scheme," *Fourth IEEE International Conference on Electronics, Circuits, and Systems* (ICECS 97), Cairo, Egypt, December 15-18 1997 (Masselos K., Kittes G., Karayiannis Y., and Stouraitis T.).
63. "Low Power Image Coding Using a Block Transformation," *Fourth International Conference on Electronics, Circuits, and Systems*, ICECS 97, Cairo, Egypt, December 15-18 1997 (Masselos K., Merakos P. Stouraitis T. and Goutis C. E.).
64. "Multiple-Valued Logic Voltage-Mode Storage Circuits Based on True-Single-Phase Clocked Logic," *Proceedings of the 8th Great Lakes Symposium on VLSI*, February 19-21, 1998, Lafayette, Louisiana, (I. Thoidis, D.J. Soudris, I. Karafyllidis, A. Thanailakis, and T. Stouraitis).
65. "A Novel Methodology for Power Consumption Reduction in a Class of DSP Algorithms," 1998 IEEE International Conference on Circuits and Systems (ISCAS'98), Monterey, California, USA, May-June 1998. (K. Masselos. P. Merakos, T. Stouraitis, C. E. Goutis).
66. "Novel Codebook Generation Algorithms for Vector Quantization Image Compression," 1998 IEEE International Conference on Acoustics Speech and Signal Processing (ICASSP'98), Seattle, Washington, USA, May, 1998. (K. Masselos, T. Stouraitis, C. E. Goutis).
67. "Low Power Implementation of Discrete Wavelet Transform," IX European Signal Processing Conference (EUSIPCO'98), Rhodes, Greece, September 1998. (K. Masselos. P. Merakos, T. Stouraitis, C. E. Goutis).
68. "A VLSI Architecture for Fast and Accurate Floating-Point Sine/Cosine Evaluation," *5th IEEE International Conference on Electronics, Circuits and Systems (ICECS'98),* Lisbon, Portugal, 7-10 September 1998. (V. Paliouras, K. Karagianni and T. Stouraitis).
69. "A Very-Long Instruction Word digital signal processor based on Logarithmic Number System," *5th IEEE International Conference on Electronics, Circuits and Systems (ICECS'98)*, Lisbon, Portugal, 7-10 September 1998. (V. Paliouras, J. Karagiannis, G. Aggouras and T. Stouraitis).
70. "Low Power Synthesis of Sum-Of-Product Computation in DSP Algorithms," 1999 IEEE International Conference on Circuits and Systems (ISCAS'99), Orlando, Florida, USA, May-June 1999. (K. Masselos, P. Merakos, T. Stouraitis, C. E. Goutis).

71. "Novel High-Radix Residue Number System Multipliers and Adders," in proceedings of *1999 IEEE International Symposium on Circuits and Systems*, Orlando, Florida, USA, Vol. I, pp. I.451 – I.454, May 30 - June 2, 1999. (V. Paliouras and T. Stouraitis).
72. "Grouped-Moduli Residue Number Systems," In proceedings of 1999 IEEE *International Symposium on Circuits and Systems*, *(ISCAS'99),* Orlando, FL, May 1999, pp. III 478 - III 483. (A. Skavantzos and T. Stouraitis).
73. "A Neural Methodology for Mapping Nested-Loop Algorithms to Heterogeneous Processor Arrays," *2nd IMACS International Conference on Circuits, Systems and Computers (IMACS-CSC'98),* Vol.1, pp. 111-115, Piraeus, Greece, October 26-29, 1998 (This paper is also included in the book "*Recent Advances in Circuits and Systems*", World Scientific Publishing Co., pp. 323-336, 1998). (K. Karagianni, A. Tzigkounakis, C. Goutis and T. Stouraitis).
74. "Defect Detection and Classification on Web Textile Fabric Using Multi-resolution Decomposition and Neural Networks," *5th IEEE International Conference on Electronics, Circuits and Systems (ICECS'99)*, Pafos, Cyprus, 5-8 September 1999 (Yorgos A. Karayiannis, Radovan Stojanovic, Panagiotis Mitropoulos, Christos Koulamas, Thanos Stouraitis, Stavros Koubias and George Papadopoulos).
75. "A novel hardware algorithm for residue evaluation," *Signal Processing Systems (SiPS 1999*), pp. 671-680, Taiwan, Oct. 1999. (K. Karagianni and T. Stouraitis)
76. "Power Analysis of the ARM7 Embedded Microprocessor," *Ninth International Workshop Power and Timing Modelling, Optimization and Simulation (PATMOS '99),* October 6-8, 1999, Kos Island, Greece (G. Synevriotis and T. Stouraitis).
77. "A Hybrid Image Compression Algorithm Based On Fractal Coding And Wavelet Transform." In proceedings of 2000 IEEE *International Symposium on Circuits and Systems*, *(ISCAS'00),* Geneva, May 2000 (I. Andreopoulos, Y. A. Karayiannis, T. Stouraitis)
78. "Low Power Synthesis of Sum-Of-Products Computation," ACM/IEEE *International Symposium on Low Power Electronic Design (ISLPED 2000),* July 2000, Portofino, Italy. (K. Masselos S. Theoharis P. K. Merakos T. Stouraitis C. E. Goutis)
79. "Logarithmic Number System for Low-Power Arithmetic". In Proceedings of *PATMOS 2000*, Sep. 2000, LNCS 1918, pp. 285-294, Springer-Verlag, 2000. (V. Paliouras and T . Stouraitis).
80. "A low-complexity RNS Multiplier," in Proceedings of *Signal Processing Systems* (*SiPS 2000*). Lafayette, USA, Oct. 2000 (V. Paliouras, K. Karagianni, and T. Stouraitis).
81. "The Impact of Arithmetic in Lowering the Chip Energy Consumption," NORCHIP 2000, Turku, Finland Nov. 2000 (T. Stouraitis)..
82. "High-radix Residue Number System Forward and Inverse Converters," *7th IEEE International Conference on Electronics, Circuits & Systems (ICECS 00),* December 17-20, 2000 Kaslik, Lebanon. (V. Paliouras and T. Stouraitis).
83. "Development Of A Power Efficient Image Coding Algorithm Based On Integer Wavelet Transform", *7th IEEE International Conference on Electronics, Circuits & Systems (ICECS 00),* December 17-20, 2000 Kaslik, Lebanon. (Masselos K., Karayiannis Y.A. Andreopoulos, I. Stouraitis, T).
84. "Signal Activity and power consumption reduction using the Logarithmic Number System," in Proceedings of *IEEE International Symposium on Circuits and Systems 2001*. Sydney, May 2001. (V. Paliouras and T. Stouraitis).
85. "A Vector Processor for 3-D Geometrical Transformations," in Proceedings of *IEEE International Symposium on Circuits and Systems 2001*. Sydney, May 2001. (K. Karagianni, T. Stouraitis).
86. "A Wavelet-Tree Image Coding System With Efficient Memory Utilization," in Proceedings of 2001 IEEE International Conference on Acoustics Speech and Signal Processing (ICASSP'01), Salt Lake City, Utah, USA, May, 2001. (Y. Andreopoulos, P. Schelkens, J. Cornellis, N. Zervas, C. Goutis, T. Stouraitis).
87. "Low-power Properties of the Logarithmic Number System," in Proceedings of *15th IEEE Symposium on Computer Arithmetic*, Vail, Colorado, 11-13 June 2001. (V. Paliouras and T. Stouraitis).

88. "Implementing Efficiently A Wavelet Transform – A Roadmap," in Proceedings of the 8th Int. workshop on Systems, Signals and Image Processing (IWSSIP 2001), *Special session on "The role of wavelets in modern multimedia standards*, Bucharest, Romania, June 7 – 9 2001, (Y. Andreopoulos, P. Schelkens, T. Stouraitis, J. Cornelis).
89. "VLSI Architectures for Blind Equalization Based on Fractional-order Statistics", in Proceedings of *8th International Conference on Electronics, Circuits, and Systems* (ICECS), Malta, September 2001. (V. Paliouras, J. Dagres, P. Tsakalides, and T. Stouraitis).
90. "A Local Wavelet Transform Implementation versus an Optimal Row-Column Algorithm for the 2D Multilevel Decomposition," in Proceedings of 2001 IEEE International Conference on Image Processing (ICIP2001), Thessaloniki, Greece, October 7-10, 2001 (Y. Andreopoulos, N. Zervas, Lafruit, P. Schelkens, T. Stouraitis, C. Goutis, and J. Cornelis).
91. "VLSI Architectures For The Implementation Of The Wigner Distribution," in Proceedings of *IEEE International Symposium on Circuits and Systems* (ISCAS) 2002. Scottsdale, Arizona, May 2002. (K. Karagianni, T. Stouraitis).
92. "A Novel List-Scheduling Algorithm For The Low-Energy Program Execution," in Proceedings of *IEEE International Symposium on Circuits and Systems* (ISCAS) 2002. Scottsdale, Arizona, May 2002. (G. Synevriotis, T. Stouraitis).
93. "Low Power Convolvers Using the Polynomial Residue Number System," in Proceedings of *IEEE International Symposium on Circuits and Systems* (ISCAS) 2002. Scottsdale, Arizona, May 2002. (V. Paliouras, A. Skavantzos, T. Stouraitis).
94. "Multi-voltage low power convolvers using the Polynomial Residue Number System," in Proceedings of *12th Great Lakes Symposium on VLSI,* April 18-20, 2002, New York City. (V. Paliouras, A. Skavantzos, T. Stouraitis).
95. "Design methodology of multiple-valued logic voltage-mode storage circuits," in *Proceedings of the 1998 IEEE International Symposium on Circuits and Systems (ISCAS '98)*, 31 May-3 June 1998, (Thoidis, I.; Soudris, D.; Karafyllidis, I.; Thanailakis, A.; Stouraitis, T.).
96. "Multiple-valued logic voltage-mode storage circuits based on true-single-phase clocked logic," in Proceedings of the 8th Great Lakes Symposium on VLSI, 19-21 Feb. 1998 (Thoidis, I.; Soudris, D.; Karafyllidis, I.; Thanailakis, A.; Stouraitis, T.).
97. "An efficient probabilistic method for logic circuits using real delay gate model," in *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems (ISCAS '99)*, 30 May-2 June 1999 (Theodoridis, G., Theoharis, S., Soudris, D., Stouraitis, T., Goutis, C.).
98. "The VLSI implementation of a baseband receiver for DECT-based portable applications," *in Proceedings of the 1999 IEEE International Symposium on Circuits and Systems (ISCAS '99),* 30 May-2 June 1999 , (Perakis, M., Tzimas, A.E., Metaxakis, E.G., Soudris, D., Kalivas, G.A., Katis, C., Dre, C., Goutis, C.E., Thanailakis, A.; Stouraitis, T.)
99. "A Computational Technique and a VLSI Architecture For Digital Pulse Shaping In OFDM Modems," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS) 2003*, May 25-28, 2003, Bangkok, Thailand. (Eleni Fotopoulou, Vassilis Paliouras, Thanos Stouraitis).
100. "A Navier-Stokes Processor for Biomedical Applications," in *Proceedings of IEEE International Workshop on Signal Processing Systems (SiPS) 2005*, Nov 2-4, 2005, Athens, Greece. (V. Zygouris, K. Karagianni, Th. Stouraitis).
101. "An RNS Architecture of an Fp Elliptic Curve Point Multiplier," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS) 2006*, May 21-24, 2006, Kos, Greece. (Dimitrios Schinianakis, Apostolis Fournaris, Athanasios Kakarountas, Thanos Stouraitis).
102. "Execution Time Comparison of Lifting-based 2-D Wavelet Transform Implementations on a VLIW DSP," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS) 2006*, May 21-24, 2006, Kos, Greece. (Konstantinos Masselos, Yiannis Andreopoulos, Thanos Stouraitis).

103. "Software-Controlled Scratchpad Mapping Strategies for Wavelet-Based Applications," in *Proceedings of IEEE International Workshop on Signal Processing Systems (SiPS) 2006*, October 2- 4, 2006, Banff, Canada. (B. Geelen, A. Ferentinos, F. Catthoor, A. Vandercappelle, G. Lafruit, T. Stouraitis, R. Lauwereins, D. Verkest).
104. "A new approach to elliptic curve cryptography: an RNS architecture," *IEEE Mediterranean Electrotechnical Conference (MELECON) 2006,* 16-19 May 2006. (Schinianakis, D., Kakarountas, A.P., Stouraitis, T.) **It won the *2nd Best Paper Award*.**
105. "Content-Adaptive Wavelet-Based Scalable Video Coding," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS) 2007,* 27-30 May 2007, Louisiana, USA (D. Athanasopoulos, T. Stouraitis).
106. "Analysis and design of a WLAN OFDM transmitter with digital filters," *Proceedings of Mobimedia 2007,* August 27-29, 2007, Nafpaktos, Greece (Eleni Fotopoulou, Thanos Stouraitis).
107. "Adaptive mapping to resource availability for dynamic wavelet-based applications," *Proceedings of ESTIMedia 2007* (V. Ferentinos, B. Geelen, F. Catthoor, A. Vandercappelle, G. Lafruit, T. Stouraitis, R. Lauwereins, D. Verkest).
108. "SOFLOPO: Towards Systematic Software Exploitation for Low-Power Designs," ACM/IEEE *International Symposium on Low Power Electronic Design (ISLPED 2000),* July 2000, Portofino, Italy. (G. Sinevriotis, A. Leventis, D. Anastasiadou, C. Stavroulopoulos, T.Papadopoulos, T. Antonakopoulos and T. Stouraitis).
109. "A Frequency-Domain Interpolation Implementation," 2008 IEEE Int. Symposium on Wireless Pervasive Computing, May 2008, Santorini, Greece. (H. Fotopoulou, V. Paliouras, and T. Stouraitis)
110. "Data Representation and Reuse in DSP Algorithms: An Ecological Dimession," *Plenary Talk,* 2008 *International SOC Design Conference*, Nov. 2008, Busan, Korea (T. Stouraitis).
111. "Low Power Data Representation in DSP algorithms," *Plenary Talk,* 2009 *CISP-BMEI International Conference*, Oct. 17-19 2009, Tianjin, China (T. Stouraitis).
112. "Power Line Communication Techniques for Coding, Modulation, and Transmission of Information in the 'Last Mile'," Proceedings of the Athens 2009 session of the Greek Committee of CIGRE, 3-4 Dec. 2009, Athens, Greece (T. Anastasselos, T. Stouraitis).
113. "Design of a Balanced 8-Modulus RNS," *Proceedings 16th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2009*, Hammamet, Tunisia, 13-16 December, 2009 (Skavantzos A., Schinianakis, D., Stouraitis, T.)
114. "Elliptic Curve Point Multiplication in GF(2^n) Using Polynomial Residue Arithmetic," *Proceedings 16th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2009*, Hammamet, Tunisia, 13-16 December, 2009 (Schinianakis, D., Kakarountas. T., Stouraitis, T., Skavantzos A.)
115. "Study, Design, and Implementation of a Variable-Wordlength IDCT processor," *Proceedings 4th Panhellenic Conference of Electrical & Computer Engineering Students,* Patra, Greece, November 19-20, 2010 (Christidis G., Stouraitis, T.)
116. "Optimal Modulus Sets for Efficient Residue-to-Binary Conversion Using the New Chinese Remainder Theorems," *Proceedings 17th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2010*, Athens, Greece, 12-15 December, 2010 (Narayanaswamy N., Skavantzos A., Stouraitis, T.)
117. "Comparison of time and frequency domain interpolation implementations for MB-OFDM UWB transmitters," in *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS) 2010,* 1-3 June 2010, Paris, France (H. Fotopoulou, D. Thanou, T. Stouraitis).
118. "A RNS Montgomery Multiplication Architecture," in *Proceedings of* the 2011 IEEE International Symposium on Circuits & Systems *(ISCAS)*, Rio, Brazil, DOI: 10.1109/ISCAS.2011.5937776 Page(s): 1167 – 1170, May 2011. (Schinianakis, D., Stouraitis, T.)
119. "GF(2^n) Montgomery Multiplication Using Polynomial Residue Arithmetic," in *Proceedings of* the 2012 IEEE International Symposium on Circuits & Systems *(ISCAS)*, Seoul, Korea, 20-23 May 2012 (Schinianakis, D., Stouraitis, T.)

120. "Hardware-Fault Attack Handling in RNS-Based Montgomery Multipliers," in *Proceedings of* the 2013 IEEE International Symposium on Circuits and Systems *(ISCAS)*, Beijing, China, 19-23 May, 2013 (Schinianakis, D., Stouraitis, T.)
121. "An RNS Modular Multiplication Algorithm," *Proceedings 17th IEEE International Conference on Electronics, Circuits and Systems, ICECS 2014*, Abu Dhabi, UAE, 8-12 December, 2014 (Schinianakis, D., Stouraitis, T.)
122. "Hardware-fault attack handling in RNS-based Montgomery Multipliers," in *Proceedings of the 2013 IEEE International Symposium on Circuits & Systems* (ISCAS), Beijing, China, 19-22 May 2013. (Schinianakis, D., Stouraitis, T.)
123. "*Cryptographic System Implementations*," The 17th CSI International Symposium on Computer Architecture & Digital Systems **(**CADS 2013), Oct. 29-31, 2013, Tehran, Iran.
124. "*An RNS Modular Multiplication Algorithm*," *IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Abu Dhabi, UAE, December 2013, (Schinianakis, D., Stouraitis, T.).
125. "An RNS Barrett modular multiplication architecture," *IEEE International Symposium on Circuits and Systems* (ISCAS 2014), Melbourne, Australia (Schinianakis D., Stouraitis T.).
126. «*Flexible Cryptographic Systems*»," The IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2014), Nov. 17-20, 2014, Ishigaki Island, Okinawa, Japan.
127. "Matching Data Representation to Application Needs - Case Study: Cryptographic Systems," Keynote Speech, 18th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS 2015) 22-24 April 2015, Belgrade, Serbia.
128. "A Reliable and Energy Efficient IoT Data Transmission Scheme for Smart Cities based on Redundant Residue based Error Correction Coding," SWANSITY 2015 - 2nd Workshop on Smart Wireless Access Networks for Smart cITY (IEEE SECON Workshop), June 22, 2015, Seattle, USA (Chinmaya Mahapatra, Zhengguo Sheng, Victor C.M. Leung, and Thanos Stouraitis).
129. "Low-Complexity Energy-Efficient Security Approach for E-Health Applications Based on Physically Unclonable Functions of Sensors", 2015 IEEE Intl Conference on Electronics, Circuits, & Systems, Cairo, Egypt, December 6-9, 2015.

Conference Session Organization

"A Reliable and Energy Efficient Data Transmission Scheme for Internet of Things based on Residue Arithmetic," submitted to 33rd IEEE International Performance Computing and Communications Conference**.**

THESES' SUPERVISION

- 8 Ph.D.s. 3 Ph.D.s are currently under supervision
- 6 Master's theses, while at Ohio State University
- 5 Master's theses at the Graduate Program on DSP systems, University of Patras
- 41 diploma theses (Master's-level, 5-year program), University of Patras